REMARKS

Examiner P. Brock II, is thanked for his thorough examination of the Prior Art, he is also thanked for his indication of allowing claims 3, 4 and 7 if these claims are rewritten in independent form including all of the limitations of the base claim and any intervening claims. Applicant has amended all claims as kindly suggested by the Examiner. Applicant has further removed objections that have been raised by Examiner from the claims and is of the opinion that, in view of the amendments that have been provided to the claims, claims 3, 4 and 7 are now acceptable. Claims 1-19, 21 have been amended.

Favorable reconsideration of this application in light of the above amendments and the following remarks is respectfully requested.

The invention teaches new method for creating an inductor on the surface of a silicon substrate. The invention provides overlying layers of oxide fins beneath a metal inductor. The oxide fins provide the stability support for the overlying metal inductor while also allowing horizontal air columns to

simultaneously exist underneath the inductor. Overlying layers of air cavities that are spatially inserted between the created overlying layers of oxide fins can be created under the invention by repetitive application of the mask used. The presence of the air wells on the surface of the substrate significantly reduces parasitic capacitances and series resistance of the inductor associated with the substrate.

Claim Objections

Claims 1-3 and 13 are objected to because of various informalities.

Applicant has carefully reviewed the claims to eliminate the informalities that have been pointed out be Examiner in addition to other's. All claims are now believed to be in allowable condition.

In light of the foregoing response, applicant respectfully requests that the Examiner's objections to claims 1-3 and 13 be withdrawn.

Claim rejections - 35 U.S.C. § 112

Reconsideration of the rejection of claims 5-9, 11, 12 and 17 under 35 U.S.C 112 as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention is respectfully requested based on the following.

The Examiner is thanked for pointing out the various antecedent basis problems in the claims. The claims have been carefully reviewed and amended to correct those problems the Examiner pointed out, in addition to others. All claims are now believed to be in allowable condition.

In light of the foregoing response, applicant respectfully requests that the Examiner's objections to claims 5-9, 11, 12 and 17 under 35 U.S.C 112 be withdrawn.

Claim rejections - 35 U.S.C. § 103

Reconsideration of the rejection of claims 1, 2, 8, 10 and 14-16 under 35 U.S.C 103 as being unpatentable over Lur et al. (US Patent 5,828,121) in view of Chu et al. (US Patent 6,140,197) is respectfully requested based on the following.

Lur et al. provides for:

- a multi-level electrode metal structure and the interconnecting inter-level metal studs used in the fabrication of VLSI circuits (ABSTRACT); Lur et al. therefore do not provide creating a high quality inductor on the surface of a silicon semiconductor substrate as claimed in claims 1, 15-18, 20 of the instant invention
- the basic and essential difference between Lur et al. and the instant invention is readily apparent by comparing Fig. 11 of Lur et al. with Fig. 13 of the instant invention: Lur et al. does provide for an dielectric of air that surrounds interconnect metal, the instant invention provides for a number of overlying air gaps that are interconnected as claimed in claims 1, 3-5, 7, 19, 21 of the instant invention
- from Fig. 11, Lur et al., it is apparent that the interconnect metal layers 29, 50, 60 and 70 are not supported by an underlying layer since the dielectric underneath these layers of interconnect metal is air; the instant invention provides oxide fins (36, 38, Fig. 13) beneath the metal inductor 44; the oxide fins provide the stability support for the overlying metal 44 while also allowing horizontal air columns to simultaneously exist underneath the inductor

- Lur et al. does not create an inductor (44, Fig. 13 of the instant invention) that overlies a upper layer of dielectric as claimed in claims 1, 15-18, 20 of the instant invention
- Lur et al. do not provide for openings (22, 24, 32 and 34, Fig. 13 of the instant invention) in layers of dielectric through which nitride or any other disposable material can be removed as claimed in claims 3, 4, 5, 7-12 of the instant invention
- Lur et al. do not provide for overlying layers of disposable material, such as nitride, interspersed with layers of dielectric as claimed in claims 1, 3-5, 7-12 of the instant invention
- the final construct that is provided by Lur et al. does not comprise horizontal air gaps (36, 38, Fig. 11 of the instant invention) between which horizontal layers of a dielectric are created, see Fig. 11 of the instant invention
- Lur et al. show interconnect studs that connect to bit lines and word line of what appears to be a DRAM circuit configuration; gate electrodes are provided by Fur et al.; the instant invention is silent on this aspect of the Fur invention and is not limited to a DRAM device or the use of gate electrodes.

Regarding claim 1, 2 the following comments apply:

- the metal layer that is created by Fur et al., layer 26, Fig. 1, is connected to a source/drain region or to a gate electrode; the metal layer of the instant invention, layer 12, is not limited to being connected to a gate electrode
- the first layers of interconnect metal, layers 40, Fig. 1, that are created by Fur et al. connect to interconnect plugs 26; the instant invention does not create these first layers of interconnect metal
- Fur et la. deposits a number of thin envelop oxide layers such as layer 42, Fig. 1, layer 42, Fig. 2, layer 42, Fig. 4, layer 42, Fig. 6, layer 42, Fig. 8, layer 42, Fig. 9, layer 42, Fig. 10; all envelop layers have been referred to by the number "42" by Fur et al., the multiplicity of layers has been deposited for the figures that have been referenced; the instant invention does not make use of such thin layers of oxide for protective purposes of the interconnect metal
- Applicant respectfully disagrees with Examiner regarding the statement that Fur et al. create, Figs. 2-4, a structure for a first layer of cavities; Fur et al. do not make use of cavities but in contract etch away the inter-level dielectric (cool. 3, line 62) leaving an air dielectric 85 between the electrode metal layers; an identical comment applies to

Examiner's contention that Fur et al. create a first and a second layer of cavities

- Chu et al. disclose forming a metal inductor on the surface of a thin layer of oxide but form, see ABSTRACT, "a plurality of openings through the intermetal dielectric layer to the semiconductor substrate"; Chu el al. therefore also does not make use of horizontal air cavities interspersed between layers of dielectric

Regarding claim 8, it is not clear to Applicant where Fur et al. refer to nitride as a disposable solid; nitride is used as a disposable solid by the instant invention, that is the invention make novel use of a characteristic of nitride. Whether Fur et al. refer to nitride as a disposable solid therefore does not distract from the novelty of the use that is made by the invention of the disposable characteristic of nitride.

Regarding claim 10, the etching of the dielectric as applied by Fur et al, col. 3, line 63, is an entirely different process than the removal of nitride or a disposable solid through a number of overlying openings that have been created in overlying layers of dielectric. For the etching of the layer of dielectric as applied by Fur et al, the surface

of the layer of dielectric that is being etched is essentially exposed, layers 34 of Fig. 10, Fur et al. This is clearly not the case for the removal of the layers of nitride of the invention, Figs. 10 and 11 of the instant invention, where the nitride layers 26 and 16 are removed through openings 32, 34, 22, 24. The process is significantly different and must therefore be claimed under the instant invention.

Regarding claim 14, Fur et al. shows, Fig. 1, gate electrodes 24, Fig. 1. Since the instant invention provides for the creation of an inductor (as opposed to interconnect metal as provided by Fur et al.), it is of significance that the inductor of the instant invention can be used as part of an oscillation circuit, which in many applications is created using CMOS devices and as part of an RF amplifier circuit.

Regarding claims 15, 16, while many inductors are created having a spiral shape, not all inductors have a spiral shape. Since the inductor of the invention is created on the surface of a layer of dielectric, layer 42, Fig. 12, the inductor of the invention is not limited to a spiral shape but can also be circular of polygonal in shape. This is specified in claims 15-17.

Regarding claim 13, it is clear that an insulation layer, as specified by Abidi et al., can be used for multiple applications. In the case of the instant invention, the insulation layer is specified and provided in order to provide a more rugged construction that is protected from environmental impact during subsequent processing cycles. Without this protective layer the inductor of the invention would be exposed and unprotected, resulting in a device that is prone to environmental damage.

Abidi et al. create an inductor over a pit in a substrate and essentially shows the inductor as having a spiral shape. Other shapes are highlighted by Abidi et al., which however does not provide any commonality between Abidi et al. and the instant invention. The essence of the instant invention is the creation of air gaps interspersed with layers of dielectric, Abidi does not address these aspects of the instant invention. It must again be pointed out that, since the inductor of the instant invention is created overlying the surface of a layer of dielectric, this inductor is not in any way limited to the shape in which this inductor can be created. For this reason the various shapes in which an inductor can be created must be specified in order to avoid incompleteness of the specification or the claims.

Regarding claim 18, the inductor of the invention is created having very low parasitic capacitance between the inductor 44, Fig. 13, and a metal layer 12, Fig. 13. For this reason the inductor can be created having a high inductive value and can at the same time be used for high frequency applications. In other words: by providing the invention it is now possible in the context of the instant invention to create a high value, high frequency inductor. The layer of material underlying the inductor is key and of the essence to these performance characteristics of the inductor. It must therefore be recognized and specified that, if an inductor is created using the instant invention, this inductor can be a high inductive value, high frequency performance inductor as claimed in claim 18. Without this claim it would not be clear just what could be accomplished using the invention.

The above arguments can be summarized by stating that it would not be obvious to combine the teachings of Lur et al. with those of Chu et al. and Abili et al., since there is no suggestion or motivation in the teachings of any of the patents of the present invention. None of these inventions provide for the creation of horizontal air gaps that are interspersed with layers of dielectric while further none of these inventions provide for a method of removal of a disposable solid, such as

nitride, for the creation of the air gaps as claimed in claims 1, 3-5, 7-12 of the instant invention. None of the applied or known references address the invention as shown in the amended claims in which air gaps are created between overlying layers of dielectric. The invention is believed to be patentable over the prior art cited, as it is respectfully suggested that the combination of these various references cannot be made without reference to Applicant's own invention. None of the applied references address the problem of creating a high inductive value, high frequency inductor overlying a layer of metal. Applicant has claimed his process in detail. The processes of Figs. 1-11 are believed to be both novel and patentable over these various references, because there is not sufficient basis for concluding that the combination of claimed elements would have been obvious to one skilled in the art. That is to say, there must be something in the prior art or line of reasoning to suggest that the combination of these various references is desirable. We believe that there is no such basis for the combination. We therefore respectfully request Examiner P. Brock II to reconsider his rejection in view of these arguments and the amendments to the Claims.

In light of the foregoing response, applicant respectfully requests that the Examiner's rejection of claims 1, 2, 8, 10 and

14 under 35 U.S.C 103 as being unpatentable over Lur et al. (US Patent 5,828,121) in view of Chu et al. (US Patent 6,140,197) be withdrawn.

The prior art made of record and not relied upon that is considered pertinent to Applicant's disclosure, that is Buynoski (US Patent 6,078,088), Thomas et al. (US Patent 5,000,818), Ahn (US Patent 6,037,248), Havemann et al (US Patent 5,936,295), Mathews (US Patent 5,171,713), Pyke (US Patent 4,671,852) have been examined and have been found to be of general interest to the invention. These prior art records however do not teach the extent and the detail combined with the flexibility of the present patent application.

Other Considerations

No new independent or dependent claims have been written as a result of this office action, no new charges are therefore incurred due to this office action.

SUMMARY

The invention teaches new method for creating an inductor on the surface of a silicon substrate. The invention provides

overlying layers of oxide fins beneath a metal inductor. The oxide fins provide the stability support for the overlying metal inductor while also allowing horizontal air columns to simultaneously exist underneath the inductor. Overlying layers of air cavities that are spatially inserted between the created overlying layers of oxide fins can be created under the invention by repetitive application of the mask used. The presence of the air wells on the surface of the substrate significantly reduces parasitic capacitances and series resistance of the inductor associated with the substrate.

It is requested that should Examiner not find the claims to be allowable that he call the undersigned Attorney at his convenience at 845-452-5863 to overcome any problems preventing allowance.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned:

"Version with markings to show changes made."

Respectfully submitted,

Stephen B. Ackerman (Reg. No 37,761)

Version with markings to show changes made

Please amend the claims as follows.

1. (Amended) A method of forming air gaps within an integrated circuit structure, comprising the steps of:

providing a partially fabricated integrated circuit structure and depositing a layer of dielectric thereon;

forming a metal layer on the surface of said dielectric layer;

depositing a thin layer of oxide over the surface of said dielectric layer thereby including said metal layer;

forming [the] a structure for a first layer of cavities over the surface of said thin layer of oxide and aligned with said metal layer, said forming a structure for a first layer of cavities comprising applying and patterning a first layer of nitride followed by applying and patterning a first layer of oxide, said forming a structure for a first layer of cavities further comprising forming a first and a second opening through said first layer of oxide;

forming [the] a structure for a second layer of cavities above and aligned with said structure for said first layer of cavities, said forming a structure for a second layer of cavities comprising applying and patterning a second layer of

nitride followed by applying and patterning a second layer of oxide, said forming a structure for a second layer of cavities further comprising forming a first and a second opening through said second layer of oxide;

creating the first and the second layer of cavities;

performing an oxide deposition over the surface of said second layer of cavities, [thereby] creating a thin layer of oxide; and

forming a metal inductor on the surface of said thin layer of oxide.

2. (Amended) The method of claim 1 wherein said forming a metal layer on the surface of said dielectric layer is forming a layer of metal that has the cross section of a square or a rectangle with essentially vertical sides whereby the height of said metal layer is equal to the thickness of a conventional semiconductor metal layer whereby [furthermore the] a width of said metal layer is equal to or exceeds its height by a measurable amount.

3. (Amended) The method of claim 1 wherein said forming the structure for a first layer of cavities comprises the steps of:

depositing a first layer of nitride over the surface of said thin layer of oxide;

creating [a] an opening in said first layer of nitride whereby said opening aligns with said metal layer and has a dimension when measured in [the] a direction along the surface of said thin layer of oxide that is smaller than [the] a dimension of the [top] surface of said metal layer by a measurable amount;

depositing a first layer of oxide over the surface of said first layer of nitride thereby including said opening in said first layer of nitride whereby said first layer of oxide has a dimension of thickness in addition to having a dimension of width; and

creating a first and a second opening in said first layer of oxide whereby said first and second openings are located at the opposite extremities of said first layer of oxide whereby the distance between the central axis of said first and second openings is less [that] than said dimension of width of said first layer of oxide by a measurable amount.

4. (Amended) The method of claim 1 wherein said forming the structure for a second layer of cavities comprises the steps of:

depositing a second layer of nitride over the surface of said first layer of oxide thereby including said first and second openings created in said first layer of oxide;

creating [a] an opening in said second layer of nitride whereby said opening aligns with said metal layer and has a dimension when measured in [the] a direction along the surface of said first layer of oxide that is approximately equal to [the] a dimension of the opening created in said first layer of nitride;

depositing a second layer of oxide over the surface of said second layer of nitride thereby including said opening created in said second layer of nitride whereby said second layer of oxide has a dimension of thickness in addition to having a dimension of width; and

creating a first and a second opening in said second layer of oxide whereby said first and second openings are located at [the] opposite extremities of said second layer of oxide whereby [the] a distance between [the] a central axis of said first and second openings is less [that] than said dimension of width of said second layer of oxide by a measurable amount.

7. (Amended) The method of claim 1, [wherein] said creating [the] a first and [the] a second layer of cavities is removing said first and second layer of nitride, said removal to take place by accessing said first and second layer of nitride by means of said first and second opening created in said second layer of oxide furthermore by accessing said first layer of

nitride by means of said first and second openings in said first layer of oxide.

8. (Amended) The method of claim 1 wherein said performing an oxide deposition over the surface of said second layer of cavities is creating a thin layer of oxide over the surface of said second layer of oxide thereby furthermore closing off said first and said second openings created in said second layer of oxide.

9. (Amended) The method of claim 1, [whereby this method is further extended to create] creating additional layers of cavities over a preceding layer of cavities, said [extension to occur] additional layers being created prior to performing an oxide deposition over the surface of [the] an upper or last layer of cavities, [whereby the] said creation of [each] additional [layer] layers of cavities [comprises] comprising the steps of:

depositing an additional layer of nitride over the surface of [the] a layer of oxide of [the] a preceding layer of cavities thereby including [the] first and second openings created in said layer of oxide of [the] a preceding layer of cavities;

creating a opening in said additional layer of nitride, [whereby] said opening [aligns] being aligned with said metal

layer and [has] having a dimension when measured in [the] a direction along the surface of said layer of oxide of [the] a preceding layer of cavities that is approximately equal to [the] a dimension of [the] an opening created in [the] a preceding layer of nitride;

depositing an additional layer of oxide over the surface of said additional layer of nitride thereby including said opening created in said additional layer of nitride, [whereby] said additional layer of oxide [has] having a dimension of thickness in addition to having a dimension of width; and

creating a first and a second opening in said additional layer of oxide, [whereby] said first and second openings [are] being located at [the] opposite [extremities] extremes of said additional layer of oxide, [whereby the] a distance between [the] a central axis of said first and second openings [is] being less [that] than said dimension of width of said additional layer of oxide by a measurable amount.

9. (Amended) The method of claim 1, [wherein] said layers of nitride [are] being [replaced by] layers of a disposable solid.

9. (Amended) The method of claim 8, [wherein] said disposable solid [layer is] being a polymer, [and whereby] said [removing said disposable solid layer] creating a first and a second layer

of cavities is heating said substrate in oxygen, [thereby] evaporating said disposable solid layer [thereby disposing the polymer] using O_2 plasma.

10. (Amended) The method of claim 8 wherein removing said disposable solid layer is introducing a solvent to said substrate, [thereby] dissolving said disposable solid layer.

11. (Amended) The method of claim 8 wherein [removing said disposable solid layer] creating a first and a second layer of cavities is heating said substrate, [thereby] evaporating said disposable solid layer.

12. (Amended) The method of claim 11 wherein [removing said disposable solid layer] creating a first and a second layer of cavities is applying a vacuum to said substrate, [thereby] dissolving said disposable solid layer.

13. (Amended) The method of claim 1 wherein [furthermore] an insulating layer is deposited over the surface of said inductor thereby encapsulating said inductor.

14. (Amended) The method of claim 1, [wherein] said partially fabricated integrated circuit structure [contains] comprising

transistors, [wherein] said transistors [are] being bipolar or CMOS devices [and are] interconnected to form and RF amplifier.

15. (Amended) The method of claim 1, [wherein] said inductor [is] being a spiral [shaped].

16. (Amended) The method of claim 15, [wherein] said spiral of said inductor [is of] being a circular or polygonal [shape].

17. (Amended) The method of claim 16, [wherein] the polygonal [shape] of said inductor [includes the shapes of] being a square[,] or a hexagon [and] or an octagon.

18. (Amended) The method of claim 1, [wherein] said inductor [has] having an inductance in excess of 1 nH and a self-resonance in excess of 10 MHz.

19. (Amended) A multilevel structure [containing] comprising horizontal air cavities in support of a metal inductor, [containing] comprising:

a semiconductor surface that has been provided with a metal point of electrical reference or that functions as an inner port on its the surface;

a thin layer of oxide overlying said semiconductor surface, [thereby] including [the] exposed surfaces of said metal point of electrical reference or inner port;

a first horizontal cavity overlying said thin layer of oxide, [whereby] said first horizontal cavity [is] being discontinued above said metal point of electrical reference or inner port;

a first layer of dielectric overlying said first horizontal cavity including said regions of discontinuance of said first horizontal cavity;

vertical openings in said first layer of dielectric [that are] located at [the near] extremities of said first layer of dielectric;

a second horizontal cavity overlying said first layer of dielectric, [whereby] said second horizontal cavity [is] being discontinued above said metal point of electrical reference or inner port;

a second layer of dielectric overlying said second horizontal cavity including said regions of discontinuance of said second horizontal cavity;

vertical openings created in said second layer of dielectric located at [the near] extremities of said second layer of dielectric; and

a thin layer of oxide overlying said second layer of dielectric.

21. (Amended) The structure of claim 19 whereby said structure is further extended to include additional layers of horizontal air cavities in support of a metal inductor, each layer containing one horizontal cavity and one layer of dielectric overlying said horizontal cavity with each horizontal cavity being discontinued above said metal point of electrical reference or inner port, [whereby furthermore] each dielectric layer [is] having been provided with vertical openings located at [the near] extremities of said layer of dielectric, said additional layers of horizontal air cavities [to be] being located underneath said thin layer of oxide overlying [the] an upper or last layer of dielectric.